## REMARKS/ARGUMENT

In the most recent Office Action, claims 1-19 were examined. Claims 1-19 are rejected. Accordingly, claims 1-19 are pending in the present application. No new matter is added. Applicants thank the Examiner for the thorough search and consideration of the invention claimed in the present application, and respond to the comments in the Office Action as follows.

**Claim Rejections - 35 U.S.C. §103**

The Office Action states that claims 16-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Miyasaka (U.S. Patent No. 6,124,154) in view of Kuo et al. (U.S. Patent No. 5,981,347). In particular, the Office Action states that the combination of Miyasaka and Kuo et al. disclose all the limitations of the rejected claims in an obvious combination. The rejection is respectfully traversed.

Applicants note that the disclosure by Miyasaka calls for a semiconductor layer that is formed as a film, and without being exposed to atmosphere, is recrystallized in a non-oxidizing atmosphere. That is, Miyasaka changed the state of the original semiconductor film to a single crystalline state, or at least modifies the polysilicon to provide a better conducting and smoother surface (col.16, line 30 - col. 17, line 7). This smooth silicon layer is very different in character from the rough polysilicon layer described in claims 16-19. That is, the electron mobility of polysilicon is roughly two orders of magnitude lower than single crystal silicon due to the change in state of the silicon lattice structure. Accordingly, because Applicants have recited a rough polysilicon layer in claims 16-19, which is not changed prior to deposition of a gate dielectric layer on top of a polysilicon layer, the disclosure by Miyasaka does not teach the limitations recited in the claims.

In addition, Applicants note that Kuo et al. appear to disclose the performing of a high temperature anneal after the formation of a gate oxide only to permit the exposed source/drain regions to be activated. That is, Kuo et al. do not teach the high temperature anneal of a gate oxide layer on a polysilicon layer, as is recited in claims 16-19, but rather appears to teach a high temperature anneal of active source/drain regions that are exposed because of the patterned gate oxide regions. Since the gate oxide regions used by Kuo et al. are for a very different purpose

(forming the source/drain regions) than for the purpose used in the present application, Applicants respectfully submit that it is not obvious to combine the disclosures by Miyasaka and Kuo et al. to arrive at the present invention, and that even if the disclosures are combined, the combined teachings still do not teach or suggest all the claim limitations recited in claims 16-19.

Indeed, if Miyasaka were to be combined with the disclosure by Kuo et al., the resulting combination would still not include the formation of a rough polysilicon layer on an insulating substrate that is then overlaid by a gate dielectric layer. At most, such a combination would provide a patterned exposure of the single crystalline layer by Miyasaka et al., or the device and procedure by Kuo et al. would be made unworkable because no source/drain regions would be exposed because of the lack of patterning taught in Miyasaka for that purpose. Accordingly, Applicants respectfully submit that even if the teachings of Miyasaka and Kuo et al. were combined, one of ordinary skill in the art would still be at a loss as to how to arrive at the present invention recited in claims 16-19. Applicants therefore respectfully request that the rejection of claims 16-19 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

The Office Action states that claims 1-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Huang et al. (U.S. Patent No. 6,037,199) in view of Doklan et al. (U.S. Patent No. 4,851,370) or Kuo et al. In particular, the Office Action states that the combination of the disclosures by Huang et al. and Doklan et al. or Kuo et al. teach all of the claim limitations of claims 1-19. The rejection is respectfully traversed.

Applicants note that, as with the disclosure by Miyasaka, Huang et al. appear to use a polysilicon layer that is converted to a single crystalline layer prior to the deposition of further layers or films. However, claims 1-19 recite the provision of a rough polysilicon layer and a gate dielectric layer either grown or deposited on the polysilicon layer. This limitation is also not shown in either Doklan et al. or Kuo et al.

Applicants further submit that it would not be obvious to combine the disclosures by Huang et al. and either Doklan et al. or Kuo et al. to arrive at the present invention recited in claims 1-19. Indeed, even if such a combination were possible, the result would still not include a polysilicon layer overlaid by a gate dielectric layer. As discussed above, Kuo et al. calls for an oxide layer for use as a mask in the formation of source/drain regions, where the underlying

silicon is exposed. This is not the case in the present application, as recited in claims 1-19 where no oxide patterning occurs before an anneal step. Applicants further note that Huang et al specifically call for a single crystalline region formed under the gate dielectric layers, which is quite different from the rough polysilicon layer formed under the gate oxide layers of the present invention. Indeed, if it were possible to combine these disclosures, the result still would not include a polysilicon layer overlaid by a gate oxide layer and would indeed result in a device that would be unworkable. That is, if Kuo et al. or Doklan et al. were combined with Huang et al., the result would be exposed areas of single crystal silicon for formation of source/drain regions, which are totally lacking in Huang et al., or the covering of source/drain regions with an oxide layer, thereby rendering them ineffective, or non-operative for the purpose for which they were intended in the disclosure by Kuo et al.

Accordingly, Applicants respectfully believe that the rejection of claims 1-19 under 35 U.S.C. §103(a) is overcome, and respectfully requests that it be reconsidered and withdrawn.

Applicants also note that the Office Action states that the disclosure by Yamazaki (U.S. Patent No. 6,306,213) discloses ranges that would have been obvious to one of ordinary skill in the art to apply to obtain the present invention. However, Applicants note that Yamazaki failed to disclose the use of a gate dielectric layer over a polysilicon layer, but rather discusses a crystallized semiconductor layer that is obtained prior to deposition of a gate dielectric layer (col. 7, line 17- col. 8, line 17). Accordingly, Applicants respectfully submit that the disclosure by Yamazaki should not be considered to teach one of ordinary skill in the art the use of an obvious range in a process in which the parameters and materials are entirely different. That is, the question of obviousness is not what is possible for one of ordinary skill in the art, but what would be suggested to one of ordinary skill in the art by the cited prior art references and knowledge available to one of ordinary skill in the art. While the disclosure by Yamazaki is not being used to reject any of the claims in the application, Applicants note that it would not be obvious to obtain the invention recited in claims 1-19 based on the disclosure by Yamazaki, either alone or in combination with the other cited prior art references.

Applicants further note that none of the cited prior art references disclose the limitations recited, for example, in claims 2, 8 and 17, wherein the polysilicon layer is recited to be of a

thickness of from about 500 to 1500Å. Applicants therefore submit that these claims at least should be allowed as reciting limitations that are neither taught nor suggested in the cited prior art references, either alone or in combination.

**Conclusion**

Applicants respectfully believe that the present response addresses all issues raised in the most recent Office Action. Applicants further submit that because there have no modifications to the claims of the application, that no further search or fact finding should be required. Accordingly, Applicants respectfully request that the present amendment be entered and considered on the merits, and that the application be passed to allowance regarding claims 1-19.

If it is believed that an interview would contribute to progress in the application, the Examiner is requested to contact the undersigned counsel at the number provided below.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 29, 2004:

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Respectfully submitted,

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